Abstracts

High-Speed GaAs Static Random-Access Memory

G. Bert, J.-P. Morin, G. Nuzillat and C. Arnodo. "High-Speed GaAs Static Random-Access Memory." 1982 Transactions on Microwave Theory and Techniques 30.7 (Jul. 1982 [T-MTT] (Joint Special Issue on GaAs IC's)): 1014-1019.

An 8-bit fully decoded RAM test circuit has been designed and fabricated using enhancement-mode GaAs-MESFET's with the LPFL circuit approach. Correct operation of the circuit has been observed for a supply voltage varying from 3.5 to 7 V. An access time of 0.6 ns was measured for a total power consumption of 85 mW under nominal operating conditions. This circuit was used to develop and validate both a design strategy and computer-aided design (CAD) tools oriented towards cache or buffer memories of realistic complexity. It is shown that a performance-optimized 1-kbit RAM exhibiting an access time of 1.1 ns for a power dissipation of 850 mW would be feasible with the present fabrication technology.

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